Siliconix

Application Note AN79-4

Driving MOSPOWER® FETs

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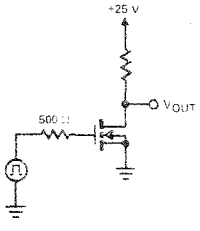
INTRODUCTION

Using VMOS Power FETs you can achieve performance never before possible–if you drive them properly. This article describes circuits and suggests design methods to be used in order to obtain the performance from VMOS that you need.

When designing with VMOS there are some facts that must be kept in mind in order to get optimum results with every circuit. The first fact is that VMOS is a very high frequency device. The cut-off frequency for all VMOS FETs is several hundred megahertz. Most power designers are not used to designing with extremely high frequency devices because with bipolars the frequency response decreases as the power increases. The very high frequency response of VMOS is the basis for many of its advantages but it must be kept in mind while designing. With improper circuit design VMOS can oscillate. This oscillation can be eliminated, though, by exercising two simple precautions. First, minimize lead and trace lengths whenever possible, especially leads associated with the gate of the FET. If it is not possible to have short leads to the gate place a ferrite bead on the gate lead or a small resistor in series with the gate. The ferrite bead or the resistor must be very close to the gate. Second, because of the extremely high input impedance of VMOS (in excess of 10^{12} Ω) drive circuits may be designed which are very high impedance. Under these conditions it is possible for the gate node to get enough positive feedback from the gate-to-drain capacitance or just from stray fields in the circuit to cause oscillation. This must be kept in mind in the design of the circuit.



A Typical VMOS Switching Circuit
Figure 1

When driving VMOS it must be kept in mind that the dynamic input impedance is very different than the static input impedance. The input of a VMOS device is capacitive. The DC input impedance is very high but the AC input impedance varies with frequency. Because of this effect, the rise and fall times of VMOS are dependent on the output impedance of the circuit driving it. The first approximation of the rise or fall time is simply

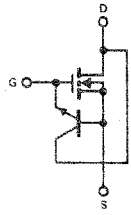
$$t_r \text{ or } t_f = 2.2 \cdot R_{OUT} \cdot C_{iss} \qquad (1)$$

where R_{OUT} is the output impedance of the drive circuit. This equation is valid only if the drain load resistance is much larger than R_{OUT}. Knowing this fact, along with the fact that there is no storage or delay time with VMOS, it is very easy to calculate the rise and fall times and set them to any desired value. For example, if you wanted to calculate the 10% to 90% rise or fall time for the circuit shown in Figure 1 using Equation 1 the rise time is equal to:

$$t_r = (2.2)(500)(50 \times 10^{-12}) = 55 \text{ nsec}$$

The dynamic input characteristics of VMOS are covered very thoroughly in Siliconix' application note AN79-3.[1]

A last thing to remember when you are driving VMOS is the input protection zener diode. When putting a positive voltage on the gate with respect to the source, the maximum voltage rating of the zener diode should not be exceeded. It is more important, however, that you do not forward bias the zener diode by putting a negative voltage on the gate while the VMOS is operating in a circuit. The reason for this is most easily explained by referring to Figure 2. As can be seen in the figure, the zener diode is actually the base-emitter junction of a bipolar transistor. If a negative voltage greater than 0.6 V is placed on the gate, the base-emitter junction of the bipolar will be forward biased which will turn on the bipolar transistor. When the bipolar is turned on, current will flow from the drain through the bipolar and out the gate. This operating condition is very likely to be destructive. If negative voltages must be placed on the gate it is recommended that you use a VMOS part that does not have an input zener diode. Non-zenered equivalents are available for most of Siliconix' zenered devices.



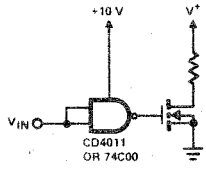
A Parasitic NPN Transistor in Zener Protected MOSFETS
Figure 2

Of all operating modes the common-source configuration is the simplest to drive. Because of the high input impedance of VMOS it can be driven directly from many logic families. When driving from a CMOS gate as shown in Figure 3, rise and fall times of about 60 nsec can be expected due to the limited source and sink currents available from the CMOS gate.[2] If faster rise and fall times are required there are several ways to obtain them. One easy way is if there are extra gates in the package that is driving the VMOS simply put the extra gates in parallel with the gate already being used. The additional current available will cut down the rise and fall times. If no extra gates are available an emitter-follower buffer can be used as shown in Figure 4. With this circuit the current available to the VMOS will be the output current of the CMOS multiplied by the beta of the bipolars. Because the bipolars are operating as emitter-followers there will still be no storage time to worry about and the frequency limit will be determined by either the CMOS gate or the f_T of the bipolars, whichever comes first.

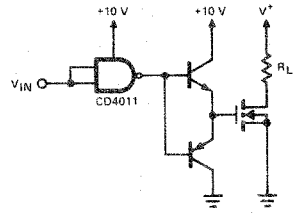
VMOS can also be driven directly from TTL gates. Because the output voltage of TTL is limited, the output current of the VMOS will be limited to some value less than its maximum rated current. The output current that can be expected can be determined from the transfer characteristic of the device being used. For example, if a TTL gate is driving VN46AF the minimum output current of the VMOS will be approximately 250 mA. This value was obtained by using the minimum output voltage of the TTL gate (3.2 V) for a high level output and referring to the transfer characteristic for the VNAZ which is the VMOS geometry used in the VN46AF. If more than 250 mA is required the output of a standard VMOS gate can be pulled up to the 5 V rail as shown in Figure 5. With a full 5 V on the gate the VN46AF will typically sink 600 mA.

For very high speeds a capacitive driver such as the MH0026 can be used as shown in Figure 6. With this drive configuration typical rise and fall times are less than 10 nsec.

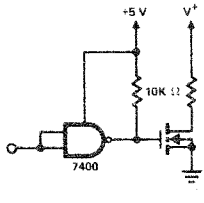
When operated in the common-drain mode VMOS is somewhat more difficult to drive than when in the common-source mode. Because of VMOS' high input impedance, though, it is considerably easier to drive common-drain than a bipolar would be when operated common collector. Common-drain circuits can be used when the load needs to be connected to ground, when an active pull-up and pull-down is required (totem pole circuit), or in bridge type circuits. For the purpose of this discussion all examples will be shown with totem pole circuits.



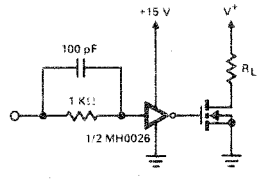
Driving VMOS with a CMOS Gate
Figure 3



An Emitter-Follower Circuit Will Decrease VMOS Rise and Fall Times
Figure 4

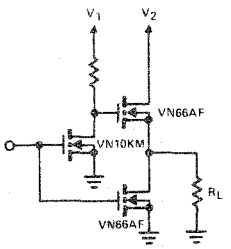


Pulling Up a TTL Output Will Increase the Sink Current of the VMOS
Figure 5



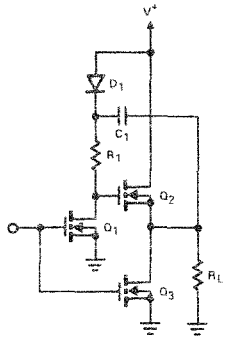
Using an MOS Clock Driver to Drive VMOS
Figure 6

The difficulty with common-drain circuits occurs because as the voltage across the load increases the enhancement voltage of the common-drain device decreases. Referring to Figure 7, as the voltage across R_L approaches V_2 the enhancement voltage for the upper VN66AF decreases. If V_1 is not greater than V_2 then the voltage across R_L can never reach V_2. For this reason whenever a common-drain circuit is used it is always necessary to have or to generate a voltage that is greater than the voltage which is desired to be impressed across the load. The amount the voltage has to be above the desired drain voltage is dependent upon the current the VMOS must source and can be determined from the transfer characteristic of the VMOS being used. If no supply voltage is available other than the one the load is to be pulled up to, one can be generated. This can be done very easily because of the very low drive current requirements of the VMOS.

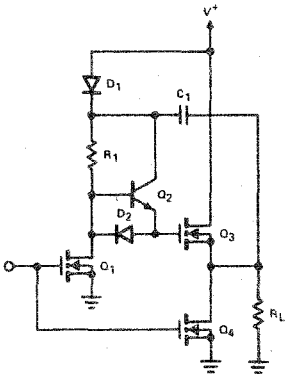


VMOS in Totem-Pole Configuration
Figure 7

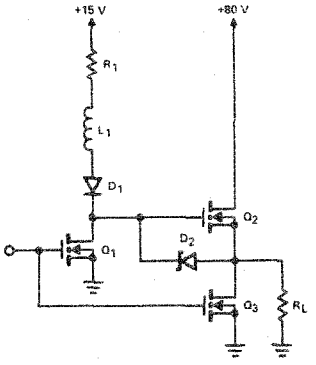
One way of generating the required gate voltage is the bootstrap circuit shown in Figure 8. In the circuit, when Q_1 and Q_3 are on, C_1 is charged to the supply rail through D_1. When Q_1 and Q_3 are turned off, the gate voltage on Q_2 goes to the supply rail. As the source of Q_2 begins to pull R_L up, the voltage across C_1 will be maintained, therefore, the gate-to-source voltage of Q_2 will be maintained. The size of C_1 should be large enough so that when it charges the gate capacitance of Q_2 a minimum voltage equal to the required enhancement voltage of Q_2 will be maintained across it. A good rule of thumb is to make C_1 equal to ten times the C_{iss} of the FET. Figure 9 shows the same bootstrap circuit with some added components to improve the rise and fall times. In the circuit Q_2 acts as an emitter-follower to increase the peak gate current to Q_3. D_2 will be forward biased when Q_1 turns on and serves as a low impedance path to discharge the gate of Q_3.



VMOS Bootstrap Circuit
Figure 8



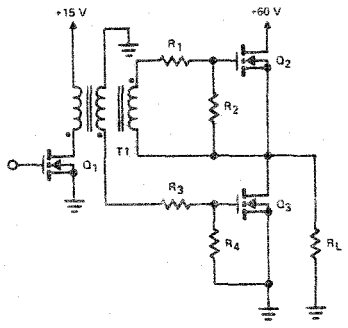
Bootstrap Circuit with Emitter-Follower for Improved Rise Times
Figure 9



Inductive Kickback Drive Circuit
Figure 10

Another method to drive a common-drain VMOS FET is shown in Figure 10. Rather than charging a capacitor and then feeding a signal back from the output as was done in the bootstrap circuit, this circuit stores the required charge in an inductor. When Q_1 is turned off a flyback voltage is generated across the inductor. This voltage is used to maintain an enhancement voltage equal to the voltage of zener diode D_2 across the VMOS FET. Once the Q_2 has been fully turned on and the voltage on R_L is at the rail a negligible amount of energy is required to keep Q_2 on. Q_2 will remain on until Q_1 is turned on, or until the leakage currents of Q_1 and D_2 discharge the gate capacitance of Q_2.

Another method that can be used to drive a common-drain VMOS is transformer drive. A transformer drive circuit is shown in Figure 11. In this circuit the transformer is used in the flyback mode when turning on the upper FET. R_1 and R_3 are used to suppress ringing and R_2 and R_4 are used to assist with turn-off of the FETs. When driving with a transformer, care must be taken to design the transformer so that the secondary inductance in conjunction with the input capacitance of the FET does not create ringing of oscillation problems.



Transformer Drive Circuit for VMOS
Figure 11

SUMMARY

The very high input impedances of VMOS Power FETs greatly simplify the drive requirements as compared to bipolars. The input drive requirements for both common-source and common-drain configurations were discussed in detail. With common-source circuits the requirement that needs to be kept in mind is the rise and fall time required. With common-drain circuits a method of maintaining an adequate enhancement voltage must be considered in addition to required rise and fall time requirements.

REFERENCES

1. A. Evans, D. Hoffman, "Dynamic Input Characteristics of a VMOS Power Switch" AN79-3.

2. D. Hoffman, L. Schaeffer, "VMOS – A Breakthrough in Power MOSFET Technology" AN76-3.